22 July '71

Dear [Name],

I made the suggestion about a month ago, and tentatively rejected it because the bits shouldn't be assigned to trivial parts of the process /O descriptors, i.e. 1 bit should suffice for the 7750 flag. I suggested:

- The 23rd bit in ECS RA is a funny one.
Re: ECS global registers & protection

The global registers work in the following way:

Bits in xo are compared with special registers in ECS controller. Earthed by having bit 23 set in xo and in ECS reg 7 (among others).

Action = read/sel/ed
If the set bits in xo are clear in registers, the bits are set in the g. register and the instruction does normal ECS read/write return. Otherwise, it does an error return.

cg. bits in g. registers ... 1100 
bits in xo 0011 
result in g. register 1111 + normal return

bits in g. registers 1100 
bits in xo 0110 
result in g. register 1100 + error return
SAD Direct
S x0 x1 ...
Rece 1
JP *
Batch count the bits
tested + an "action"
number decoded by global
register keyword

Also of interest: Selective Clear
q. reg = 1100
x0 = 101
q. reg (result) = 1000

Suggested use:

F = P. rehead
T = process timer
S = schedule data
E = event channel queueing words
16 = allocation block

Anyone who wants to touch a
"protected" data or object of
above type must successfully do
an appropriate "read/lock"
before it starts and a "selective clea"
when it is done.
MICRO which loops until it succeeds in a test-and-set action on the global register

GLBCHK where where is addressing a word which will be placed in xo

USER xo, b1x1, a6, x6, b2, b3

GLBCHK MACRO WHERE
LOCAL SETLOCK, SETUP, GLBLIST, GLBLFAIL
LOCAL PPSETUP, PWAIT, FIN
SA1 WHERE
BXO X1
SB2 1

SETLOCK SXL6 1
SA6 ILOCK

SETUP SA1 IWAIT
N2 X1 PPSETUP
SB3 GLBLOOP

GLBLIST KE 1
JP GLBLFAIL
JP FIN

GLBLFAIL SB3 B3-B2
NE B3, B0, GLBLIST
JP SETUP

Jasetup SXL6 0
SA6 ILOCK
SB3 PPULoop
PPUWAIT  S03  B3-B2
NE  B3, B0, PPUWAIT
JP  SETXOCLK
FIN  BSS  0
ENDM