

6400 Multiplexor

Reference Manual

Berkeley Computer Center

HES

REFERENCE MANUAL FOR THE BERKELEY COMPUTER CENTER MULTIPLEXOR

CONTENTS

- 1 Introduction
- 2.0 General Programmers Interface
- 3.0 Multiplexor Design
 - 3.1 Module Interface
 - 3.2 Data Flow
 - 3.3 Addressing System
- 4.0 Mechanical Construction
- 5.0 Card Notation
- 6.0 Cage Layouts
- 7.0 Initial Address Allocation**

Introduction

A large number of teletype units and other devices will be attached to the CDC 6400 computer. The basic interface to the peripheral computer of the 6400 is expensive, but has a high capacity. The multiplexor will have a single 6400 channel interface and connect to a large number of devices. It is being designed on a modular basis, so that it is easy to increase the number of slow external devices as needed. This design approach will make it more expensive but more versatile than a custom designed unit, or one using a central shared store.

The entire multiplexor hardware system has component parts as follows:

- 1) Level changing circuits to change the external device levels to those of the Fairchild logic. This also includes local and safety controls which may be considered part of the device.
- 2) Serialiser Units. These take the incoming signals and convert them to parallel form. They also provide enough bufferage to ensure that a 2 ms. response will suffice. The exact form of a serialiser is tailored to the device that is using it, but it is connected by a regular interface to the central multiplexor unit.
- 3) Central Multiplex Unit. This will determine the highest priority transfers needed and transfer between the appropriate serialiser unit and central buffer registers. Flags will indicate to the computer program when the central buffers need emptying or filling, and periodic attention by the peripheral processor program will ensure this is done.

The structure of the device from a programming point of view is that of a store of up to 512 registers to which information can be read or written, together with a ready system to avoid unnecessary seeking instructions. Most devices will have a control bit so that the program can selectively ignore their ready signals.

PROGRAMMER'S INTERFACE

An entire channel and peripheral processor are expected to be assigned to the multiplexor. If other synchronisers are attached to the same channel, the multiplexor must be last as it does not relay signals. The multiplexor responds only to the following function codes and will be disconnected by an inactive pulse from the programme.

The functions to which the multiplexor responds are:

7774 } Read up to three words from the multiplexor.
7775 }
7776 } Word 1 is control information.

2 is address in the multiplexor of device selected, the least significant bits giving the address.

3 is data from device selected.

7763 } Transmit two words to buffer.
7773 }
7767 } Word 1 is the device address in the multiplexor.

Word 2 is data for the device.

7777 Exchange data with the multiplexor. (Mainly intended for test purposes.)

Word 1 is the device address in the multiplexor.

Word 2 is data for the device.

The device is read from and filled in one operation. The data read from the device will be read eventually by 7774. The program will have to await write buffer empty, then read ignoring associated address.

As each function is completed an inactive pulse must be sent to the multiplexor to release it. See CDC input output specifications.

When reading, either one, two, or three words may be read from the multiplexor. The act of reading the second word*empties the multiplexor

*As seen from the PPU.

buffer if the read buffer was full. No more than three words should be read. The control word (first word read) has bits which indicate:

- (a) whether there is valid data to be read ($2^0=1$ if ready)
- (b) whether the write buffer is free ($2^1=1$ if busy)
- (c) whether the valid data came from a high writing address ($2^2=1$)

NOTE: Other bits of the control word may be specified later, hence their values should not be assumed.

TELETYPE MODULES (8 Bit Codes)

Data read from the device is $X_{11} \dots \dots \dots X_0$

where ~~$X_0 = 1$ if ready was set~~

(i.e. unless exchange function has just been used.)

$X_7 - X_0$ = character bits $d_7 - d_0$. ?

X_8 = 0 unless the line is broken

X_9 = one if character emptying was overdue, or if the device was unsynchronised.

If the line is broken characters consisting of ones will appear until the input is disabled. (approx. one character each 95 milliseconds)

The read address is n . The device may be ignored by sending a word with $X_{11} = 1$ to address n . After master clear the device will be ignored. The output may be mixed with the input data by sending a word with $X_{10} = 1$ to n .

The write address is $n+256$. The output to be sent is $X_0 - X_{11}$ where

$$X_0 = 0$$

$$X_1 = 1$$

$X_2 - X_9$ = bits of character (order to be determined)

$$X_{10} = 0$$

$$X_{11} = 1$$

↑ Same as input ↑
RS 9/20/67

NOTE:

a single ready is generated for each character output, and no disable is

Ⓐ needed as no readies are generated when no characters are being output.

Ⓑ For output, if power on for at least $1/10$ second then deadstart master clear, no readies will be generated.

OVERALL DESIGN OF THE MULTIPLEXOR

The central part of the multiplexor communicates with a channel and the serialisers. There are buffers for data and an address from a PPU. When loaded from the PPU the data buffer ^{is} serially emptied to the specified address. When data is emptied from one of the serialisers into the read buffer, the PPU can then read it. The high speed logic of the multiplexor is slaved to and directly controlled by a PPU and will simply gate data in and out along 12 parallel buses. It will also set 3 control flip flops namely: Read buffer empty, Write buffer full, and exchange needed.

The serial control logic will interpret these three control flip flops and serially fills or empties the appropriate buffers.

The logic has been split into six data routing cards each holding 2 bits of all the parallel registers and all identical, and ^{one} card for the high speed logic and one for the slow speed serial logic.

Module Interface

Each module communicates with the control part of the multiplexor by five signals.

X_i
 \bar{Y}_i \bar{Y}_i is inverted and gated with X_i to form an address selection signal g .

outbus. This is the 'ready' signal and the serial output. The design of the module be such that it is set to 1 only when selected.

ser This is the input serial signal. It is only other than 1 when **g is present**. It is used to load any needed shift registers from the **central** multiplexor. It is sampled at the trailing edge of sh.

sh This is a shift control pulse. The back edge is used for shifting.

ser and sh must be gated by g so that other module signals are ignored.

Data Flow and Operation

3.2

There are five 12 bit registers.

- 1 Catch register CR. This is used to extend a 25 nanosecond pulse from the PPU.
- 2 A peripheal address register PA. This is loaded from CR and can be connected to the address decoder. Only 9 bits are likely to be used.
- 3 A data shift register PD . This holds data from the peripheal. It is loaded in parallel and emptied serially, *which also clears it.*
- 4 A serial to parallel data register SD. This is loaded serially and copied in parallel to the PPU. This is also used to generate a mask and **serially gate** into the generated address register.
- 5 An address **generator register**. This can be gated to the decoder, together with a mask. It is set one digit a time -- however it is not a shift register.

There is a two-way gate to the address decoder. Either PA or GA and SD as a mask are gated to the decoder. There is a three-way gate connected to the cable-driver circuits which send data to the PPU. First, control data; second, generated address; third, SD.

SYSTEM SKETCH

Basic system takes an 8 bit address and generates ^{waveforms on} 16 X and 16 Y selection wires. Each ^{serialiser} unit takes a single X_i and a single Y to ^{that} select unit.

To select a unit which is ready we use the same decoding tree as follows: A typical unit is selected by $a_0 \bar{a}_1 a_7$. If we replace \bar{a}_1 by b_1 the decoder tree has now 16 independent inputs.

Set $a_i = 1$ and $b_i = 1$ All units are selected and the output will be the 'or' of all readyies.

Now set $a_0 = 0$ $a_1 - a_7 = 1$ and $b_i = 1$

We have generated the 'or' of $\frac{1}{2}$ the readyies and this will indicate if any ready has $a_0 = 0$ as the most significant bit. If there is a ready set $a_0 = 0$ and $b_0 = 1$, if there is no selected ready set $a_0 = 1$ & $b_0 = 0$ and a_1 accordingly and now set $a_1 = 0$. This will tell us if a_1 can be 0 for a ready signal.

Thus we can obtain the address digits one at a time. The ready with the lowest address number will thus be selected.

This simple system has the drawback that 256 elements are switched simultaneously, giving about an amp of pulse ^{current} current. This may trigger or affect the ^{RTL} circuits with their low noise margin.

To alleviate the possible trouble we arrange

- 1) local amplifiers so that most of the pulse current is local.
- 2) arrange that Y signals are inverted. This needs a number of extra inverters,

but the currents remain roughly balanced.

Similarly the two control signals (serial input and shift) are distributed to all units. These are balanced by sending one -ve to

each unit and using one inverter to obtain true signal. The relay boards are used for local amplification of the gating and other signals. They also mix the serial outputs and gate them -- an extra precaution against large circulating current loops. They also gate $\overline{\text{ser}}$ and sh, to reduce the chance of noise generation.

Address Decoding Layout

There are three registers from which addresses are derived.

- 1) PA This is set by the PPU under the control of a program
- 2) GA This is generated in response to a ready signal
- 3) SD This is used in the generation of an address to supply a bi sequence as described above.

These are gated on the 6 data routing boards and sent to 3 address decoder boards. The address decoding boards each do an initial decoding and produce 8 powerful semidecoded signals. Each relay board was 10 of these signals and decodes them further to produce 8 selection signals. Pairs of these selection signals are decoded finally on the 16 serialiser addresses controlled by the relay board.

Suitable back wiring will enable.

2	decoder boards to service 256 addresses.
3	512
6	1024

with no extra stages of decoding needed. The current back wiring is for 512 addresses.

Mechanical Construction and General Layout.

The greater part of the system will be constructed with Fairchild elements 900, 914, and 923. These are integrated RTL circuits.

Cards.

A group of such elements is mounted on a card or board. Each card has 60 positions, six rows of 10 numbered from 10 - 69 in which the elements -- or other components may be mounted. The card has a connector of 44 pins of which 32 are used for logic signals and the others used for power and grounding. In addition up to 8 test points may be provided as a maintenance aid.

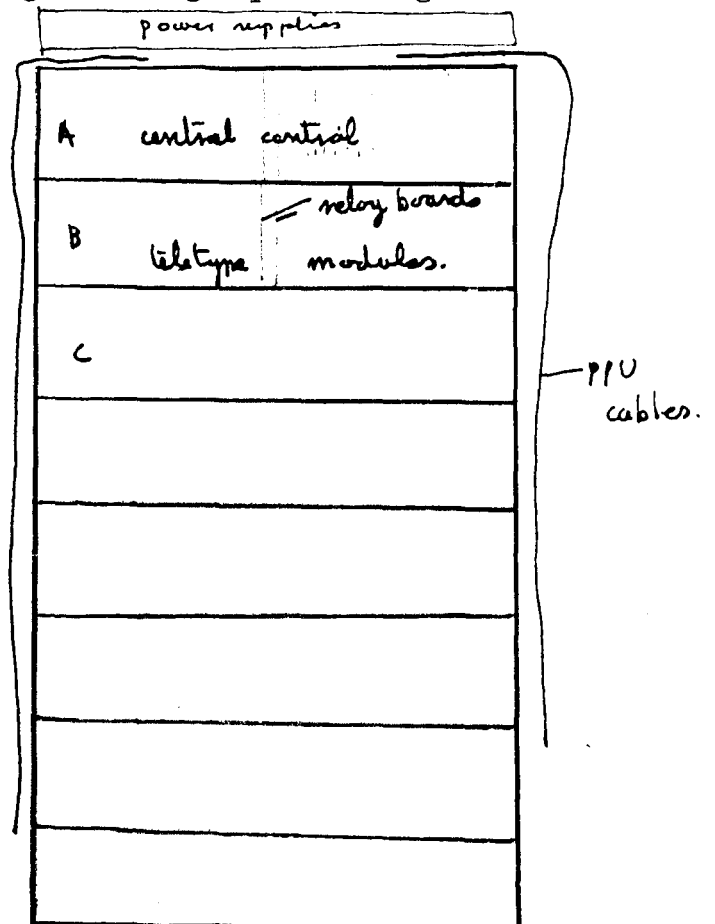
Cages.

Each cage has 27 positions numbered 1-27 in which cards may be inserted. the spacing is $1\frac{1}{2}$ times the minimum width to give ample room for components on the cards.

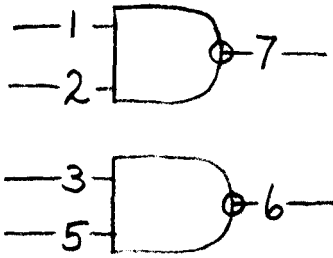
Rack

A rack will contain up to 8 logic cages two cage spaces being used for power supplies.

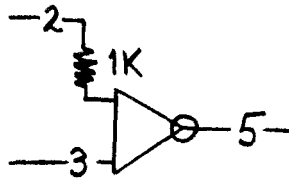
Rack Layout



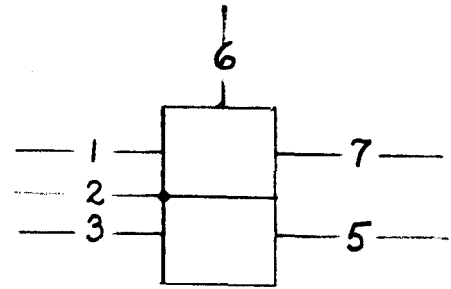
Fairchild 914



Fairchild 900



Fairchild 923



Truth Tables:

PIN	914			900		923					
	1	2	7	3	5	6	2	1	3	7	5
	(3)	(5)	(6)								
	H	H	L	H	L	L	H→L	H	H	7	5
	L	H	H	L	H			H	L	H	L
	H	L	H					L	H	L	H
	L	L	H					L	L	5	7
						H				L	H

Fanout:

IN	1,2,3,5 = 3	3 = 6	1,3,6 = 3
OUT	7,6 = 16	5 = 80	2 = 5 ; 7,5 = 10

with 2 outputs joined of a 914

fanout = 30

with $p = 1$ or $2 =$ no. of powered circuits

$n =$ no. of connected outputs

fanout = $16 P - 2n + 2$

Card Layout

Each card has 60 positions in which elements may be maintained. They are numbered from 10 - 69 in 6 rows of 10. The connector pins are numbered 1-22 and A-Z. Upto 8 test points may be mounted on a card, numbered T1.....T8. Six pairs of connector pins are used for power. Usually numbered pins are used for inputs and lettered pins for outputs. The exception is the address decoder board.

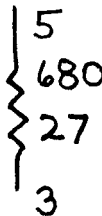
Diagram Notation

Power lines are $\left. \begin{matrix} 6F & 0V & 5E & 3.6 & 7H \\ 17U & & 18V & -6 & 16T \end{matrix} \right\}$ spare

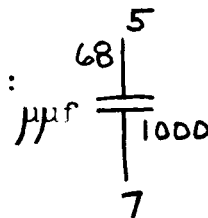
Pins of connectors \textcircled{E}

Test Points \rightarrow
T5

resistors:
values in ohms



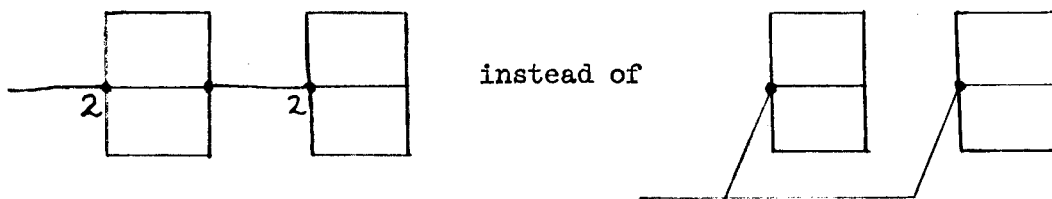
capacitors:
values in μuf

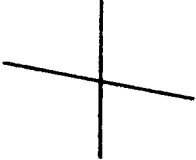



Card positions in cages are numbered from 1-27

These are cages lettered A B C D E F G H etc.

Drawings of 923 are abbreviated as follows:



Wires crossed on drawings  are supposed not to intersect
(all joins are T joins.)

Remote connections are sometimes drawn  with two arrows pointing and named.



Each card has its 3.6 volt power supply decoupled by a choke.

and each ^{used} power supply further decoupled by capacitors .01 μF & 50 μF .

Physical LocationsAddresses

	<u>read</u>	<u>write</u>	<u>devices</u>
<u>Cage B.</u>	240-255	496-511	16 teletypes.
<u>Cage C.</u>	208-233	464-479	16 1050's
<u>Cage D.</u>	144-151	400-407	8 fast lines read. 8 fast lines write (2400 bits/sec.).

EXTRA PAGES FROM MUX MANUAL

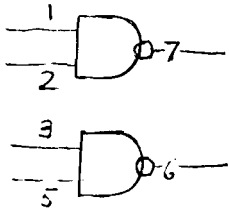
SAVE

Card Diagram Notation

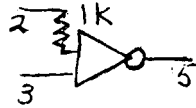
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5.6

Fairchild 914

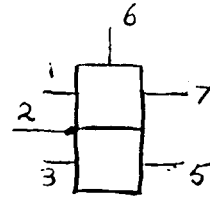


Fairchild 900



Fairchild 923

manuscript)



TEST POINT



connector pin



Truth Tables

	914			900		923					
pins:	1	2	7	3	5	6	2	1	3	7	5
	8	5	6	H	L	L	H → L	H	H	7	5
	H	H	L	L	H			H	L	H	L
	L	H	H					L	H	L	H
	H	L	H					L	L	5	7
	L	L	H			H				L	H
	<u>Fan Out</u>										
in	2	3	5	= 3	3	= 6	1, 3, 6	= 3			
out		7	6	= 16	5	= 80	2	= 5			
							7	5	= 10		

w. 2 outputs joined of a 914

fanout = 30

w. $p = 1$ or 2 = no of powered circuits

$n =$ no of connected outputs

$$n_{out} = 16p - 2n + 2.$$

Card Layout

Each card has 60 positions in which elements may be mounted.

They are numbered from 10 - 69 in 6 rows of 10.

The connector pins are numbered 1-22 and A-Z

upto 8 test points may be mounted on a card, numbered T1 --- T8.

Six pairs of connector pins are used for power.

Usually numbered pins are used for inputs and lettered pins for outputs.
 one exception is the address decoder board.

Diagram Notation

Power lines are

Pins of connectors

Test Points

Card positions in cages are numbered from 1-27

These are cages lettered A B C D E F G H etc.

Drawings of 923 are abbreviated as follows:

instead of

Wires crossed on drawings are supposed not to intersect

all joins are T joins.

Remote connections are sometimes drawn

with two arrows pointing and named.

Each card has its 3.6 volt power supply decoupled by a choke.

and each ^{used.} power supply further decoupled by capacitors .01 μ F & 50 μ F.

Diagram Notation

(Duplicated from original manuscript.)

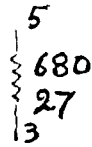
5015

power lines are. 6 F 0V 5E 3.6 7 H } spare.
 17 U 18V -6 16 T }
 Pins of connectors (E)

Test Points

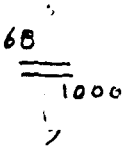


Resistor
 value in ohms



Capacitors

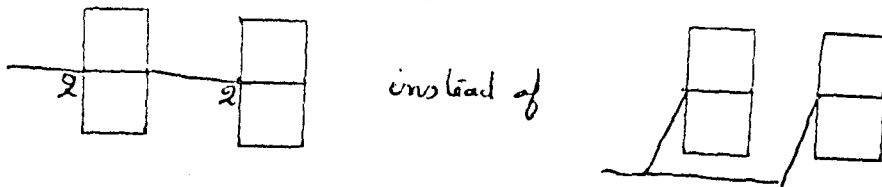
values in μF



Card Positions in cages are numbered from 1 - 27

There are cages lettered A B C D E F G H etc.

Drawings of 993 are abbreviated as follows.



Wires crossed on drawings  are supposed not to intersect.
 (air joins are T joins.)

Remote connections are sometimes drawn
 with two arrows pointing and named.

